

REMARKS

Claims 2 and 21 have been canceled, and claims 1 and 20 have been amended. Figure 8 has been amended editorially. Support for this amendment to Figure 8 is found on page 21, lines 3-6 of the specification.

Claims 1, 3, 4, 14 and 15 stand rejected under 35 U.S.C. §102(b) as being anticipated by Gould et al. (USP 5,051,917). Claims 2, 5-9, 11-13 and 16-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gould et al. Claim 10 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Gould et al. as applied to claim 2 above, and further in view of Kitamura et al. (USP 4,811,073). Claims 20-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gould et al. in view of Applicant prior art Figure 2. These rejections are respectfully traversed for the following reasons.

One of the features of the present invention pertaining to a semicustom IC lies in the architecture capable of executing modifications of cell arrangements, wirings, and circuits easily on a semiconductor chip and achieving the shortening of the development period. Namely, the claimed semicustom IC has a plurality of cell rows, in each row a plurality of standard cells are arranged, and gate array basic cells formed in an empty space of a predetermined cell row of the plurality of cell rows. The standard cells are configured to be rectangular pattern regions having a predetermined height and different widths so that the standard cells include first and second type cells. And further, each of the basic cells is configured to be a rectangular pattern region having a height substantially identical to said predetermined height and a width equal to the width of the first type cell, and not equal to the width of the second type cell. Namely, the width of the first type cell of the standard cell is equal to that of the basic cell, but the width of the second type cells may be wider and/or narrower than that of the basic cell. By this cell architecture, it is possible to execute easily circuit modifications such as the increase/decrease of driving capability of

the circuit, or the increase/decrease of power consumption, etc. in the circuit so as to manufacture semicustom ICs in a short period of time.

Turning now to Gould et al., there is no disclosure or suggestion of cells configured to be rectangular pattern regions having different widths so that the standard cells include first and second type cells. In addition, Gould et al., fail to show or suggest basic cells configured to be rectangular pattern regions having a width equal to the width of the first type cell, and not equal to the width of the second type cell. As shown in Figs. 1 and 6 of Gould et al., all of the standard cells 22 and 58 have a same width. Further, basic cells 54 and 56 are formed in locations where the standard cells are not formed (See column 4, lines 27-32, column 6, lines 19-22) so as to have a same width as that of the standard cells. That is, Gould et al. fails to teach or suggest the claimed second type cells.

On the contrary, as shown in Figs. 3A to 3D of the subject application, the claimed standard cells SC₁, SC₂, ... SC₅ include the first and second type cells, having different widths so as to arrange various circuits in respective standard cells SC₁, SC₂, ..., SC₅ to allow various functions, respectively. If the width of the standard cells is equal to the width of basic cell, as disclosed by Gould et al., the automatic arrangement by CAD methodology is very easy, because the exchange is very easy between the standard cell and the basic cell. But, as per the teachings of the present invention, if the width of the standard cells include different values then the width of basic cell, the automatic arrangement by CAD methodology becomes very complicated and difficult, because the exchange between the standard cell and the basic cell is not allowed and thus the present invention would not be obvious to one of ordinary skill in the art in view of Gould et al.

Gould et al. substantially differs from claimed structure and cannot achieve the effectiveness of the claimed invention, which allows a wide variety of circuit functions, further increasing a freedom of design of wiring so as to improve the performances of the semicustom IC.

The proposed combination of Kitamura et al., and Gould et al. does not cure the deficiencies in Gould et al., since Kitamura et al. only disclose a gate array and fail to show or suggest the claimed mixed structure of basic cells and the standard cells.

Similarly, the proposed combination of Fig. 2 of the present invention, Kitamura et al. and Gould et al. does not cure the deficiencies in Gould et al., since Fig. 2 fails to show the claimed mixed structure of basic cells and the standard cells.

Consequently, in light of the above explanation, the present application is believed to be in condition for formal allowance and an early and favorable action to that effect is requested.

Respectfully submitted,



Johnny A. Kumar
Reg. No. 34,649

October 27, 1999

Date

FOLEY & LARDNER
3000 K Street, N.W.
Suite 500
Washington, D.C. 20007-5109
(202) 672-5300